ISL5239EVAL1 Evaluation Kit

The ISL5239EVAL1 is an evaluation kit for the ISL5239 Pre-Distortion Linearizer (PDL). The kit consists of an evaluation Circuit Card Assembly (CCA) complete with the ISL5239 device and additional circuitry to provide for control via a computer USB port. Windows based demonstration software is provided for full user programmability and control of all ISL5239 operational modes. The evaluation board provides digital outputs which are accessible through standard logic analyzer headers and differential analog outputs via SMA connectors. Documentation includes full evaluation board schematics and PCB layout materials.

Matlab utility programs have been developed and are available to aid in characterizing the Power Amplifier (PA) and to facilitate programming the device Look-Up Table(s).

Features

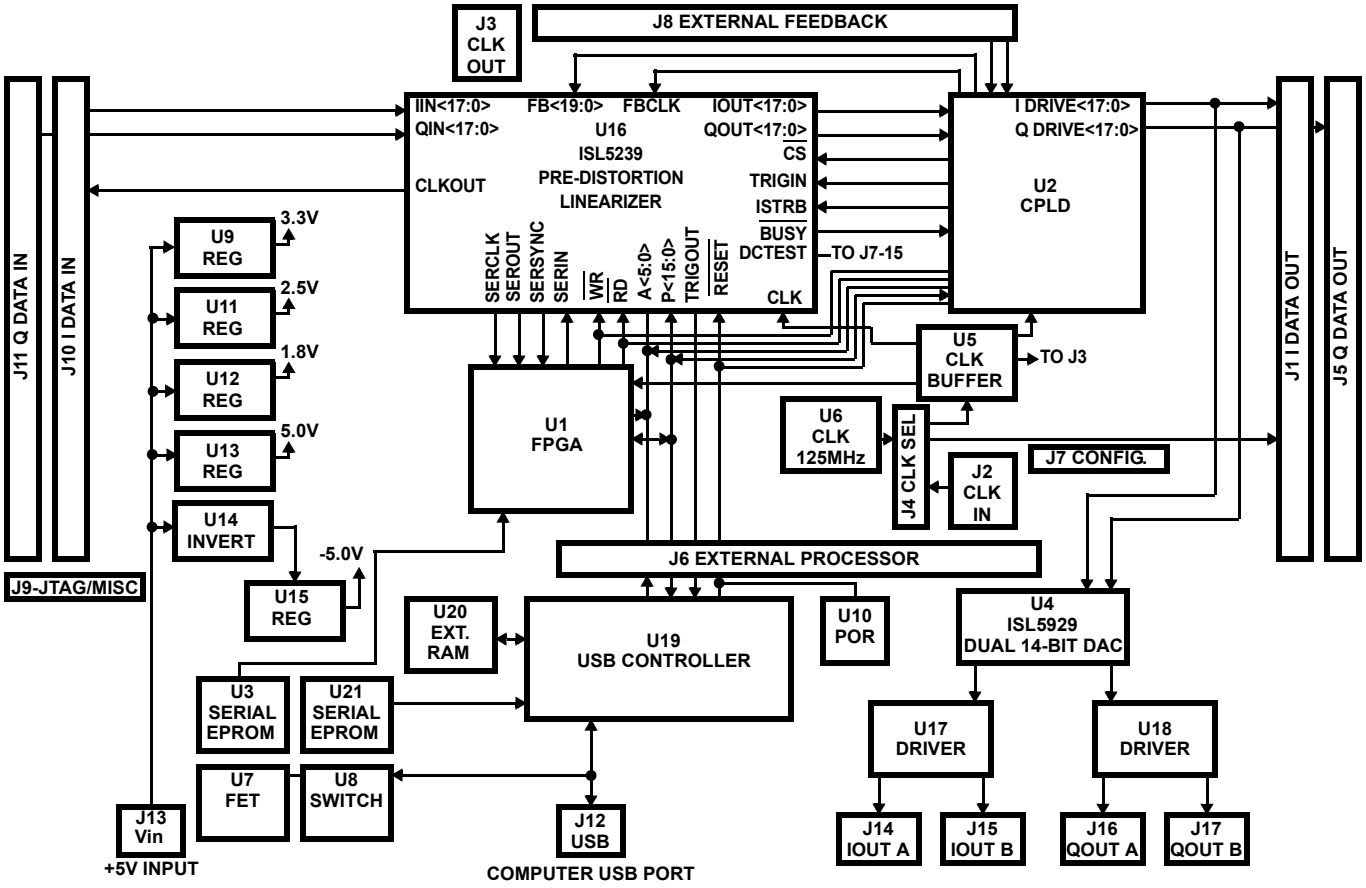
- Evaluation CCA complete with ISL5239 Pre-Distortion Linearizer and ISL5929 Dual 14-bit TxDAC
- Simple operation from a PC USB interface with Windows Based GUI software or Matlab drivers
- Example Matlab routines for PA Linearization
- Designed for compatibility with the ISL5217, ISL5216, and ISL5416 eval. boards.

Reference Documents

- ISL5239EVAL1 Software
- ISL5239EVAL1 Schematics
- ISL5239EVAL1 Layout
- ISL5239EVAL1 Bill of Material

The latest version for all reference materials and programs is available via the Intersil internet website at www.intersil.com.

Block Diagram



Getting Started

Hardware Requirements

1. A personal computer with a minimum Pentium II, 300 MHz, 32MB RAM, 5MB free disk space, v1.1 USB port interface, and running Windows 98, ME, or 2000 operating systems. Windows NT does not support the USB interface and should not be used.
2. A 5Vdc power supply capable of supporting the evaluation CCA by sourcing 2.0 amps.

Software Installation

1. In order to supply the latest software and documentation at the time of purchase, the software media is only available from the Intersil website at www.intersil.com. Please search on the device or evaluation board number, as the software and all other related documentation for the evaluation kit is downloadable from the website.
2. Download the ISL5239.exe file to the host computer's root directory. (C:)
3. Execute the 'ISL5239.exe' installation program from the distribution media. This program will create folder ISL5239 and install the required files.

Hardware Description

The ISL5239 eval. board allows demonstration of the ISL5239 device functions and can serve as a reference for development and verification of customer prototypes. In addition, the eval. board has interfaces that allow interconnection with other Intersil eval. boards and commercial equipment, as depicted in the block diagram. These interfaces facilitate the generation and observation of pre-distorted signals in a lab environment during application development to provide for PA pre-distortion algorithm development and implementation.

The device input capture memory and output capture memory provides for demonstration of the ISL5239 signal processing modes. It can be used as a device learning tool and as part of lab prototype set-up for experimental development of linearization systems. It is a tool for the early development of control set-ups, algorithms, thermal memory effect compensation, and system performance estimates.

Board Components

The evaluation board consists of four major components as depicted in the block diagram:

1. ISL5239 U16: This is the Pre-Distortion Linearizer device. This device is clocked by the onboard U6 oscillator or an external reference supplied through J2 to drive the U5 programmable skew clock buffer.
2. USB Interface U19: This is a complete USB interface to provide for programming and controlling the ISL5239 device. The USB also allows for direct configuration of the on-board CPLD and FPGA devices.
3. CPLD U2. The primary function of the CPLD is input/output signal conditioning to provide for digital output from the ISL5239 IOUT<17:0> and QOUT<17:0> output busses. The CPLD also provides several operational modes to control the FBCLK and FB<19:0> inputs.
4. FPGA U1: The FPGA's main function is to provide a user programmable hardware implementation for temperature compensation. A typical implementation is pre-loaded into the board with the details available in the device verilog.

USB Registers

The USB is configured with 128 registers which contain the control information for the CCA. These registers can be accessed from the evaluation software using the console commands "read" and "write" or the script commands "PDP.read" and "PDP.write." For more details refer to the Software Description' section.

Hardware Configuration

Verify the following default jumper configurations.

1. J4 in position 2-3, J7 5-6 and J7 7-8 jumpered.
2. Connect the 5 volt power supply to the evaluation board connector J13 utilizing the supplied power cable. Ensure the power supply can source 2.0 amps regulated at 5Vdc±5%.

WARNING: Ensure care is utilized to prevent the application of reverse polarity power to the CCA.

3. Connect the supplied USB cable from the PC's USB port to the evaluation board's J12 connector.

Software Description

The evaluation software provides a Graphical User Interface (GUI) that allows full control over all operational modes of the ISL5239 evaluation board and the ISL5239 IC. The software also implements functions for loading LUT patterns into device memory and for supporting capture memory loading and reading operations. Control of the on-board CPLD and FPGA can be accomplished via the GUI.

Controlling the board can be done by using the forms provided in the software, by using the active command window to execute commands pertaining to accessing registers directly in a peek/poke manner, or by running configuration files. The software contains eight forms, each controlling a specific part of the board.

The software also has pull-down menus through which the user can execute various commands. These commands include running configurations files, controlling the stimulus, loading the capture memories, and writing to the LUT's in the device. These functions are discussed in more details in the following sections.

Running the Software

1. Turn on the power supply to the board and verify less than 1.5A is being drawn.

2. Select and execute the ISL5239 software.
3. Modify the device parameters as required to obtain the desired configuration and performance.
4. The active window will display the execution results of the selected configuration tab, with changes shown in white and then back to green as they are implemented in the hardware.

Controlling the ISL5239

Software Forms

The software provides eight different forms for controlling the ISL5239 device. These forms can set or clear various register bits, and load associated memories. For more information concerning the interpretations of the bit fields inside these forms, refer to the ISL5239 data sheet. Table 1 describes the forms and which registers and functions are available.

TABLE 1. Software Form Definitions

FUNCTION	REGISTER ADDRESS (0Xxx)	TYPE	DESCRIPTION	ADDITIONAL FUNCTIONS
Global Control	00	R/W	Chip Control	-
	01	R	Chip ID	-
Input Formatter	02	R/W	Control	
	03	R	Status	
Capture Memory	04	R/W	Control	Memory Direct Write (Poke)
	05	R/W	Length of Input Memory Loops	
	06	R/W	Input Memory Capture Mode and Trigger Delay	Actions - Manual Trigger Actions - Idle
	07	R/W	Operating Modes	
	08	R/W	Feedback Memory Capture Mode and Trigger Delay	Capture - Configure Capture Capture - Save Feedback Capture Capture - Save Input Capture
	09	R/W	Magnitude Threshold Minimum Value	
	0a	R/W	Magnitude Threshold Maximum Value	
	0b	R/W	Memory Address	
	0c	R/W	Memory Data LSW	Stimulus - Load Stimulus Stimulus - Configure Stimulus
	0d	R/W	Memory Data MSW	
	0e	R	Input Memory Status	
	0f	R	Feedback Memory Status	

TABLE 1. Software Form Definitions

FUNCTION	REGISTER ADDRESS (0Xx)	TYPE	DESCRIPTION	ADDITIONAL FUNCTIONS
Pre-Distorter	10	R/W	Control	
	11	R/W	Magnitude Function Control	
	12	R/W	Magnitude Function Scale Factor	
	13	R/W	Look-Up Table Control	LUT Direct Write (Poke) LUT 0 - Load LUT 1 - Load LUT 0 - Save LUT 1 - Save
	14	R/W	Look-Up Table Delta Imaginary Data	
	15	R/W	Look-Up Table Delta Real Data	
	16	R/W	Look-Up Table Imaginary Data	
	17	R/W	Look-Up Table Real Data	
	18	R/W	Memory Effect Control	
	19	R/W	Memory Effect Coefficient A	
	1a	R/W	Memory Effect Coefficient B	
	1b	R/W	Memory Effect Power Integrator LSW	
	1c	R/W	Memory Effect Power Integrator MSW	
	1d	R	Status	
IF Converter	20	R/W	Control	
	21	R	Status	
Correction Filter	28	R/W	Control	
	29	R/W	Coefficient Index	
	2a	R/W	Coefficient Value	Coefficient Direct Write (Poke) Coefficients - Load Coefficients - Save
	2b	R	Status	
Output Converter (Output Data Conditioner)	30	R/W	Control	
	31	R/W	I-to-I (hm) Coefficient	
	32	R/W	Q-to-I (km) Coefficient	
	33	R/W	I-to-Q(Im) Coefficient	
	34	R/W	Q-to-Q (gm) Coefficient	
	35	R/W	I-Channel DC Offset MSW	
	36	R/W	I-Channel DC Offset LSW	
	37	R/W	Q-Channel DC Offset MSW	
	38	R/W	Q-Channel DC Offset LSW	
	39	R	Status	
Register	-	R/W	-	Register Direct Read (Peek) and Write (Poke) operations to the Eval. board registers.

CPLD Operational Modes:

The CPLD is controlled with five addressable registers.

TABLE 2. CPLD Register Description

Address (hex)	Bit-width	Read/Write	Description	Function
0x40	8	Read Only	Version Description	Returns current revision level of the CPLD programming when Peeked.
0x41	8	Read Only	Device ID Register	Returns the device ID when Peeked.
0x42	8	Read Only	Status Register	MPI I/O implemented. Register currently not used.
0x43	8	Read/Write	Configuration Register 0	Lower 4 bits assigned to Feedback Sample Selector. MPI I/O implemented; core function not implemented
0x44	8	Read/Write	Configuration Register 1	Selects the output which is routed back in to FB<19:0> and the signal source for FBCLK. See Table 3 for additional details.

There are eight CPLD operational modes selectable in control word 0x44. These modes are as shown in Table 3 and control the input source for FB<19:0> and FBCLK.

TABLE 3. CPLD Feedback Operational Modes

0x44	Source for FB<19:0>	Source for FBCLK
0x00 (default)	Hi-z	Hi-z
0x01	IOUT<17:0>	CPLD_CLK0 (system clock)
0x02	QOUT<17:0>	CPLD_CLK0
0x03	IOUT<17:8>,QOUT<17:8>	CPLD_CLK0
0x04	Connector J8 (Ext. FDBK)	$\overline{\text{J8-19}}$
0x05	Connector J8 (Ext. FDBK)	J8-19
0x06	Connector J8 (Ext. FDBK)	CPLD_CLK0
0x07	Connector J8 (Ext. FDBK)	$\overline{\text{CPLD\_CLK0}}$

CPLD and FPGA Programming

The evaluation board contains two programmable devices which are configured to support normal device evaluation and operation. These devices can be modified and re-programmed to meet a user's needs via the a JTAG programming interface J9. U2 is a Xilinx XC95288XL-6PQ208C CPLD, and is required for basic board functions. U3 is a Xilinx XC18V01VQ44C SPROM which supports optional FPGA functions. The Verilog for both of these devices is downloadable from the product page for the evaluation board, and the devices can be re-programmed utilizing the following general instructions.

CPLD U2

1. Install the parallel port JTAG programming cable XILINX Model Number DLC5, Parallel Cable III from the computer parallel port to the ISL5239EVAL1 connector J9 as follows:

- TMS to J9-7
- TCK to J9-9
- TDI to J9-12
- TDO to J9-14
- VCC to J9-19
- GND to J9-20.

2. Launch the Xilinx Device Programming iMPACT software or any similar device programming software.
3. Select 'cancel' on the 'Operation Mode Selection' dialog box.
4. Apply power to the CCA.
5. Right click on the main screen and select 'Initialize Chain.'
6. This will identify the device and pop-up a file selection window. Navigate to the desired .jed file.This will allow the JTAG Programmer to display the TDI - device - TDO chain, specifying .jed file as the programing file.
7. Highlight the XC95288XL with the cursor, right click, and select 'Program.' In the Program Options dialog box, check 'Erase Before Programming' and 'Program', then 'OK'.
8. Verify all programming actions are completed successfully. Troubleshoot the J9 JTAG to U2 path if programming is unsuccessful.

FPGA U1

1. Install the parallel port JTAG programming cable XILINX Model Number DLC5, Parallel Cable III from the computer parallel port to the ISL5239EVAL1 connector J9 as follows:

- TMS to J9-7
- TCK to J9-9
- TDI to J9-16
- TDO to J9-18
- VCC to J9-19
- GND to J9-20.

2. Launch the Xilinx Device Programming iMPACT software or any similar device programming software.
3. Select ‘File’ and then ‘Initialize Chain.’
4. This will identify the device and pop-up a file selection window. Navigate to the desired .mcs file. In the ‘Select Prom Part Name’ dialog box, select ‘xc18v01_vq44,’ and then ‘OK’. This will allow the JTAG Programmer to display the TDI - device - TDO chain, specifying the .mcs file as the programing file.
5. Highlight the XC18v01 with the cursor, right click, and select ‘Program.’ In the ‘Program Options’ dialog box, check ‘Erase Before Programming’ and ‘Program’, then ‘OK’.
6. Verify all programming actions are completed successfully. Troubleshoot the J9 JTAG to U3 path if programming is unsuccessful.
7. Select File, then Exit to complete the programming operations.
8. Remove power from the CCA.
9. Remove the serial port programming cable from connector J9.

Eval Board Timing

The CPLD and FPGA load files constrain the devices to particular timing parameters which are a function of the configuration. The timing for the supplied CPLD is as constrained in the programming files and as shown in Table 4. Additional timing information can be obtained by review of the design utilizing Xilinx ISE or other CPLD programming tools.

TABLE 4. CPLD Timing

Parameter	Symbol	Min	Max	Units
EXTERNAL CLOCK IN (J2)Frequency	FCLK	-	125	MHz
EXTERNAL CLOCK IN (J2)Period	TCLK	8.0	-	nS
EXTERNAL CLOCK IN (J2) duty cycle @ 125 MHz		50% - 200	50% + 200	pS
Delay from REF CLOCK OUT (J3) to CLOCK OUT (J10-19) in x1 mode			7.0	nS
Delay from REF CLOCK OUT (J3) to CLOCK OUT (J10-19) in x2, x4, or x8 mode			8.0	nS
Setup Time from IDATA IN<17:0> (J10) to REF CLOCK OUT (J3)		2.0		nS
Hold Time to IDATA IN<17:0> (J10) from REF CLOCK OUT (J3)		2.0		nS
Setup time from QDATA IN<17:0> (J11) to REF CLOCK OUT (J3)		2.0		nS
Hold Time to QDATA IN<17:0> (J11) from REF CLOCK OUT (J3)		2.0		nS
REF CLOCK OUT falling edge (J3) to IDATA OUT<18:0> (J1) Delay			4.0	nS
REF CLOCK OUT falling edge (J3) to QDATA OUT<18:0> (J5) Delay			4.0	nS
EXT FEEDBACK IN<19:0> (J8) to EXT FDBCK CLK (J8-19) Setup Time		2.0		nS
EXT FEEDBACK IN<19:0> (J8) from EXT FDBCK CLK (J8-19) Hold Time		2.0		nS

Internal vs. External Clock Drive

The ISL5239 is supplied with an on-board 125 MHz oscillator in position U6. The board can also utilize an external clock source through connector J2. Jumper J4 provides for the selection of either clock source, with the default position J4 2-3 selecting the on-board U6 oscillator.

Digital vs Analog Outputs

The ISL5239 outputs are available in either digital or analog format. Connector J1 can be utilized for IOUT<17:0> and connector J5 for QOUT<17:0> in digital format selectable as either 2's complement or Offset binary. The analog representation of these output is generated via U4, an ISL5929 Dual 14-bit converter. The ISL5239 drives a differential conversion and filtering network designed to directly interface with available analog quadrature modulators devices. An application note is available for additional details on the characteristics of the analog output functions.

Internal vs External Processor Control

The on-board USB controller is the primary computer interface for controlling the ISL5239. Both this GUI and the Matlab drivers are designed for operation with the USB controller. J6 can be utilized to provide for external processor control by directly connecting a host processor to this header pin interface.

GUI vs Matlab Control Interface

There are two command and control interfaces supported by the ISL5239Eval1. The GUI is a Windows based interface implemented from C source code. An additional control interface is available which allows device reads and writes from Matlab. Please see the application notes on open loop and closed loop characterization for additional descriptions of the Matlab based interfaces.